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| EXAMINER | |
|---|---|
| TU, CHRISTINE TRINH LE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2117 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/780,878 | MOTIKA ET AL. | |
| | Examiner | Art Unit | |
| | Christine T. Tu | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19-21 and 26-29* is/are pending in the application.

4a) Of the above claim(s) *22-25* is/are withdrawn from consideration.

5)☒ Claim(s) *26-30* is/are allowed.

6)☒ Claim(s) *1,6,7,9,11-13 and 17-20* is/are rejected.

7)☒ Claim(s) *2-5, 8, 10, 14-16 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/6/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-19, 20-21, and 26-30, drawn to by using a clock signal and the second clock signal, an electronic circuit testing apparatus and a method thereof for at least one of testing, diagnosing and monitoring an operation of an electronic circuit, classified in class 714, subclass 733.

II. Claims 22-25, drawn to an electronic circuit (in detail) comprising a scan chain of latches and each of the latches comprises a master flipflop and a slave flipflop, classified in class 714, subclass 726.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because an electronic circuit of group II has novelty other than the use in an apparatus or a method such that the electronic circuit of group II is being tested/monitored. The subcombination has separate utility such as being used in any other apparatus wherein data signal sequence is necessary.

The examiner has required restriction between combination and subcombination inventions. Where applicant elects a subcombination, and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

3. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art due to their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

***Response to Arguments***

5. Applicant's arguments filed April 4, 2007 have been fully considered but they are not persuasive.

Applicant argues that selectively choosing language of claims at two different levels of scope within two sets of claims and ignoring claim language at one level within one of the two sets constitutes an improper evaluation procedure both for purpose of classifying two different claim sets and for purpose of restricting between the two claim sets. Examiner, however, disagrees to applicant's remark.

As referring to Group I (claims 1-21 and 26-30), the invention is recited with the feature of monitoring/testing an electronic circuit having a clock signal and a second clock signal (two clock signals) and the feature of performing/executing a BIST sequence on the electronic circuit. Such limitations are not recited in Group II.

Even though the dependent claims (claims 4 and 29) are recited with a master flip-flop and a slave flip flop. Applicant should aware what is actually being claimed. Base on claims 4 and 29, the limitations of "...interconnects **a** (single) master flip-flop and **a** (single) slave flip-flop in latch**es** that comprise said scan chain" [in claim 4] and "(plurality) latch**es** comprise **a** (single) master flip-flop and **a** (single) slave flip-flop"[in claim 29] are recited. In other words, only a single master flip-flop and only a single slave flip-flop among plurality of latches. Therefore, only a single master flip-flop and only a single slave flip-flop are recited in the scan chain. Such limitation of a **single** master flip-flop and a

**single** slave flip-flop in a scan chain is not recited in Group II (see explanation for Group II below).

Moreover, claims 20-21 have nothing to do with any scan chain. What is being recited is the testing/diagnosing/monitoring an operation of an electronic circuit (only) with two clock signals and the feature of performing BIST sequence on the electronic circuit.

Therefore, Group I (claims 1-21 and 26-30) does belong to class/subclass 714/733—Built-in testing circuit.

For group II (claims 22-25), however, is being recited with limitation of a (plain) scan chain comprising latches and each of the latches comprising a master flip-flop and a slave flip-flop.

Firstly, in claims 23 and 25, since each of the latches (in the at least one scan chain) comprises a master flip-flop and a slave flip-flop, then plurality of master flip-flops and plurality of slave flip-flops are being recited in a scan chain. Such **plurality** of master flip-flops and **plurality** of slave flip-flops are not recited in Group I.

Secondly, such a scan chain (in Group II) can be used for any environment that is not limited to being tested or being controlled by two clock signals (a "clock signal" and a "second clock signal" as being recited in Group I). For example, a scan chain could have been used for generating test data patterns. Therefore, invention of Group II (claims 22-25) is classified in class/subclass 714/726—scan path/chain.

Base on the explanation above (¶s 1-3 and 5 above), claims 1-21 and 26-30 of Group I and claims 22-25 of Group II do have different limitations from each other. As a result, search invention in Group I does not need to search plurality of master flip-flops and plurality of slave flip-flops in a scan chain (as being recited in the invention of Group II). In addition, searching invention for Group II does not need to search the feature of testing/diagnosing/monitoring an electronic circuit using two clock signals with performing/executing a BIST sequence (as being recited in the invention of Group I). Therefore, each of the groups (Group I and II) is directed to an independent and distinct matter. The restriction still stands as in the previous office action (mailed April 2, 2007).

6. **THIS RESTRICTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Applicant elected Group I (claims 1-21 and 26-29 (as stated in the Response filed April 4, 2007).

8. Claims 22-25 (Group II) have been withdrawn.

9. In order to expedite the prosecution for the subject application, the non-elect4ed claims (claims 22-25) should be cancelled in response to this office action.

10. Claims 1-21 and 26-30 (Group I) have been examined.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 1, 6-7, 9, 11-13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Attaway et al. (5,701,308).

Claim 1:

Attaway discloses the invention substantially as claimed. Attaway teaches (figures 6 and 4) a test system containing multiple ICs, each of which having a BIST architecture as shown in Figure 4. The test system also comprises a clock multiplexer (70) for replacing a system clock (CLK) with a test clock (TCLK) based on the state of a signal on a line (RUN_TEST) (not shown) (figures 4 and 6, column 3 lines 60-62, column 10 lines 13-39).

Attaway does not explicitly teach repeatedly cycle through a predetermined cycle of operation of the circuit. Attaway, however, teaches using the test clock, the operations of loading, shifting, and sampling of test data may be perform on the ICs.

It would have been obvious to one skilled in the art at the time the invention was made to name Attaway's combination of loading, shifting and sampling operations as "repeatedly cycle through a predetermined cycle of operations". One having ordinary skill in the art would be motivated to do so because based on the recited limitation, there is no particular operation being claimed.

Claim 6:

Attaway further teaches a RAM BIST circuit (in a IC) receives test data or instructions on line TDI and then provides an output signal to an output multiplexer (22) (column 8 lines 27-34).

Claim 7:

Attaway's SCANOUT output enables signature comparison to performed by a comparator located external to the IC (column 8 lines 50-54).

Claim 9:

Attaway discloses the invention substantially as claimed. Attaway teaches (figures 6 and 4) a test system containing multiple ICs, each of which having a BIST architecture as shown in Figure 4. The test system also comprises a clock line (CLK), a test clock line (TCLK) and a clock multiplexer (70). The clock multiplexer (70) replaces a system clock (CLK) with a test clock (TCLK) based on the state of a signal on a line (RUN_TEST) (not shown) (figures 4 and 6, column 3 lines 60-62, column 10 lines 13-39).

Attaway does not explicitly teach an interrupt signal line. Attaway, however, teaches the clock multiplexer (70) replaces a system clock (CLK) with a test clock (TCLK) (column 10 lines 22-27)

It would have been obvious to one skilled in the art at the time the invention was made to name Attaway's clock multiplexer (70) as an "interrupt signal line". One having ordinary skill in the art would be motivated to do so

because naming Attaway's clock multiplexer as an "interrupt signal line" does not affect the performance of Attaway's multiplexer (70).

Claim 11:

Attaway shows a RUN_TEST line for controlling the clock multiplexer (70) (column (column 10 lines 22-27).

Claims 12-13 and 17:

Claims 12 and (13 & 17) are rejected for reasons similar to those set forth against claims 6 and 7, respectively.

Claims 18-19:

The signature comparison is used for determining the presence of faults in the scan chain of the IC (column 13 lines 8-14).

Claim 20:

This claim is similar to claim 1 except that the features are being written into a program/software which being embodied into a signal-bearing medium. Attaway teaches an external controller provides a control signal that generates instructions for an interface on the IC (column 3 lines 15-23).

14. Claims 2-5, 8, 10, 14-16 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Claims 26-30 are allowed.

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571) 272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christine T. Tu
Primary Examiner
Art Unit 2117

May 10, 2007